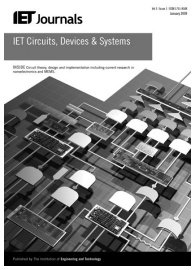
Published in IET Circuits, Devices & Systems
Received on 10th May 2012
Revised on 28th December 2012
Accepted on 9th February 2013
doi: 10.1049/iet-cds.2012.0126



ISSN 1751-858X

Analysis and design of monolithic resistors with a desired temperature coefficient using contacts

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Abstract: A technique for implementing monolithic resistors with a desired temperature coefficient (TC) over a wide temperature range is introduced. A typical monolithic resistor consists of a core resistive layer terminated with contact layers on each end. In a typical process, there are core resistive layers that have TCs with opposite sign of that of the contacts. The authors propose to take advantage of this property and distribute a certain number of contacts across the core resistor to achieve a desired overall TC for monolithic resistors. This TC can be negative, zero or positive. The methodologies for designing such resistors are presented. As a proof-of-concept, several resistor structures have been designed and implemented in a 0.13 μm complementary metal-oxide semiconductor technology. The simulation and measurement results over the temperature range of 25–200°C confirm the validity of the proposed technique.

1 Introduction

Monolithic resistors are among the essential components for many analogue and mixed-signal integrated circuits [1–4]. In particular, temperature-independent resistors, resistors with zero temperature coefficient (Z-TC), improve the reliability of such circuits for applications requiring operation over a wide range of temperature; for example, automotive, aerospace, oil, pulp and paper, and food-related applications. In addition, being able to design a resistor with a known (and desired) temperature coefficient (TC) provides more flexibility in the design of circuits for temperature-concerned applications. There are many analogue and mixed-signal integrated circuits that require temperature-independent resistors. Examples include voltage and current references and bias circuits, in particular, constant-g_m biasing in both regular and high-temperature circuits [5–12]. Resistors with a known TC can be used for temperature measurement and/or calibration.

1.1 Current approaches

There are several approaches available to implement a (near) Z-TC resistor. Some are intended for discrete (off-chip) resistors, or use non-standard materials and/or extra process steps to realise a composite on-chip resistor with Z-TC [13–18]. In addition to these approaches, there are several circuit techniques to implement (near) Z-TC resistors [19–21]. One technique is to apply an external compensation circuit [22], which requires extra design effort and circuit components. Another circuit technique is based on using two different types of monolithic resistors, negative TC (N-TC) and positive TC (P-TC) resistors [23–28]. By properly combining these resistors in series and/or parallel, a (near) Z-TC composite resistor is realised. However, in such resistor structures the effects of contacts on the temperature behaviour of the overall resistor has not been considered. The effects of contacts become more pronounced as the number of resistors that are being combined increases.

To alleviate the above-mentioned issues, the presented technique is based on implementing a given resistor using a combination of same-type resistors and considering the temperature behaviour of contacts used in sub-resistors. A preliminary concept of such technique is discussed in [29]. In this work, we expand the concept, simplify the design strategy, provide the design methodologies and verify the proposed techniques using simulations as well as measurements on a wide range of fabricated resistors. Using the proposed model, one can lay out a resistor with a controlled TC by combining several core resistors and adding certain number of contacts (with opposite TC as compared to the core resistors). Thus, a resistor with a desired TC (with negative, nearly zero or positive value) can be implemented.

In the following sections, we present the proposed monolithic resistor structure and a design strategy on how to implement a resistor with a desired TC. The proposed technique is simple and practical. Without loss of generality, we present the design technique for resistors with near Z-TC; however, the technique can be used to design resistors with a desired TC.

As a proof-of-concept, several resistor structures based on the proposed technique in the range of 1–100 kΩ have been simulated and implemented in a 0.13 μm complementary metal-oxide semiconductor (CMOS) technology. These different resistors are designed to show the impact of each

model parameter on temperature behaviour of the overall resistor. The simulation and measurement results over the temperature range of 25–200°C confirm the validity of the proposed technique. These results will be discussed in the measurement section.

2 Monolithic resistor structure

Typically, in a monolithic design, it is desirable to implement resistors with a near zero (or with a given) TC using the foundry provided resistor structures available in a given technology. Let us first briefly overview a generic resistor structure that is provided by foundries.

2.1 Foundry-provided resistor parameters

A typical resistor structure, for example, a poly resistor, consists of two physical parts, namely, a core resistor, with the sheet resistance R_{core}, and two terminal contact resistors, each one denoted as R_{cnt}. The total value of the resistor, R_{tot}, is given by

$$R_{\text{tot}} = \left(R_{\text{core}} \times \frac{L}{W}\right) + \left(2 \times \frac{R_{\text{cnt}}}{W}\right) \tag{1}$$

where L and W are the length and width of the resistive layer, for example, poly, in μm. The core resistor, R_{core}, is in Ω/sqr; each contact resistor, R_{cnt}, is in Ω·μm and total resistor, R_{tot}, is in Ω. A typical minimum value (scaled version) of L and W for such resistor, in the technology that we used, is 1.6 and 0.4 μm, respectively. Each resistor component has its own resistivity value and TC. These values are provided by the foundry. Note that to avoid disclosing the values provided by the particular foundry used in this work, the values shown in Table 1 are scaled.

As can be seen from the table, R_{core} has a P-TC and R_{cnt} has an N-TC, therefore, by proper choice of areas for the core and contact regions, one can implement a resistor with a given TC. This is the fundamental idea behind this work, which will be elaborated in more detail in this paper.

2.2 Definitions

For the purpose of clarity and brevity of the analysis that will follow, we define three unit resistors. Unit R_{core}: $R_{u.\text{core}} = R_{\text{core}} \times L_{\min}$, Unit R_{cnt}: $R_{u.\text{cnt}} = 2 \times R_{\text{cnt}}$ and Unit R_{tot}: $R_{u.\text{tot}} = R_{\text{tot}} \times W_{\min}$. Note that the factor of 2 is included in $R_{u.\text{cnt}}$ to account for the contacts at both ends of the core region. Also, note that all these defined parameters have the same unit, that is, Ω·μm. The scaled values of these parameters are also listed in Table 1. Using these three defined unit resistors, we can rewrite (1) as follows

$$\frac{R_{u.\text{tot}}}{W_{\min}} = \frac{R_{u.\text{core}}}{W} + \frac{R_{u.\text{cnt}}}{W} \tag{2}$$

Furthermore, without loss of generality, we consider the following two configurations for implementing a given resistor, R_{tot}: one resistor configuration is based on a long minimum-width core resistor with contact areas at each end, R_{long}, and the other one is a series of several short minimum-length minimum-width core resistors each having two contacts at their two ends, R_{short}. As presented in [29], any arbitrary resistor, R_{tot}, can be realised using a series combination of one $R_{\text{long}}(x)$ and one $R_{\text{short}}(n)$, as shown in Fig. 1, as follows

$$R_{\text{tot}} = R_{\text{long}}(x) + R_{\text{short}}(n) \tag{3}$$

where n is a positive integer, which is the number of series resistors in R_{short}; x is a positive real value, which is a length factor, that is, $L/L_{\min}$, where L is the length of the structure and $L_{\min}$ is the minimum length allowable in the process.

Note that since R_{core} has a P-TC and R_{cnt} has an N-TC (refer to Table 1), for a given n, by increasing x the sensitivity of R_{long} to temperature (namely, its $(\text{d}R/\text{d}T)$) increases. By proper choice of x, one can design a resistor in which core and contact resistors have the same absolute value of $(\text{d}R/\text{d}T)$, however, with opposite signs.

2.3 TC considerations

Consider a minimum-size resistor with $L_{\min}$ and $W_{\min}$ and corresponding contacts at each end, as shown in Fig. 1*a*. From Table 1, we obtain the ratio of $R_{u.\text{cnt}}/R_{u.\text{core}}$, which is equal to 86.4Ω·μm/435.2Ω·μm = 0.199. Note that for this particular case, the contact resistor is almost a fifth of the core resistor (that is, $R_{\text{cnt}} \simeq 1/6 \times R_{\text{tot}}$ and $R_{\text{core}} \simeq 5/6 \times R_{\text{tot}}$). On the other hand, the TC ratio for the R_{cnt} and R_{core}, that is, $\text{TC}_{\text{cnt}}/\text{TC}_{\text{core}}$, is –976/61.6 = –15.84. Hence, the overall TC of a minimum-size resistor R_{tot} is

Table 1 Example parameters of a specific resistor (R_{tot}) based on core resistance (R_{core}) and contact resistance (R_{cnt})

Definition	Constant	Value	Unit
minimum length	$L_{\min}$	1.6	μm
minimum width	$W_{\min}$	0.4	μm
core resistor	R_{core}	272	Ω/sqr
contact resistor	R_{cnt}	43.2	Ω·μm
core resistor-TC	TC_{core}	+61.6	ppm/°C
contact resistor-TC	TC_{cnt}	–976	ppm/°C
$R_{u.\text{core}}$ (Unit R_{core})	$R_{\text{core}} \times L_{\min}$	435.2	Ω·μm
$R_{u.\text{cnt}}$ (Unit R_{cnt})	$2 \times R_{\text{cnt}}$	86.4	Ω·μm
$R_{u.\text{tot}}$ (Unit R_{tot})	$R_{\text{tot}} \times W_{\min}$	$0.4 \cdot R_{\text{tot}}$	Ω·μm

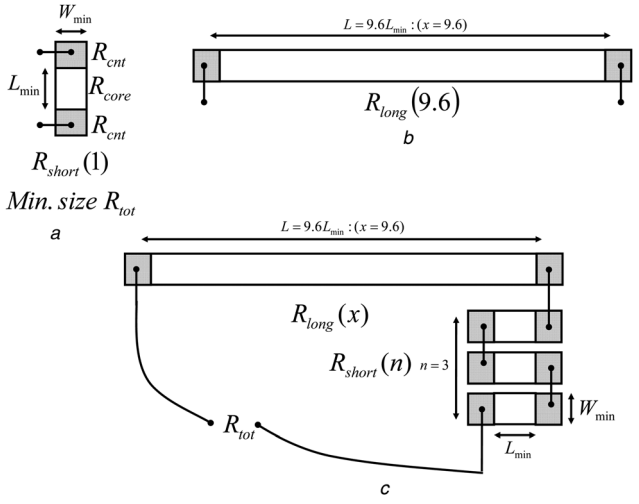

Fig. 1 *Example resistor realizations*

a Minimum-size unit resistor with $n = 1$, $L_{\min}$ and $W_{\min}$
b R_{long} with a length factor, $x = 9.6$
c R_{tot} example; series combination of n minimum-size unit resistors as R_{short} with $n = 3$ and a R_{long} with a length factor, $x = 9.6$

doi: 10.1049/iet-cds.2012.0126

mainly affected by R_{cnt}, that is, the effect of contact resistor TC on overall TC of the minimum-size resistor is approximately $-15.84 \times 0.199 = -3.15$ times more than that of the TC of core resistor.

Now, consider the case when R_{tot} is larger than the minimum-size resistor, that is, $x > 1$. We want to investigate the temperature behaviour of R_{tot} for different values of x. Based on the result of previous paragraph, if x is chosen to be around 3.15, the overall temperature dependence of the total resistor R_{tot} is proportional to $3.15 \times 5/6 = 2.63$ related to R_{core} and $-15.84 \times 1/6 = -2.64$ related to R_{cnt}. Thus, by proper choice of x, these two values can ideally cancel out each other to achieve an R_{tot} with a (near) Z-TC.

Hence, for a given R_{tot}, depending on the value of the length factor, x, one can obtain different TCs. In our example, if x is chosen to be around 3.15, a (near) Z-TC resistor will be achieved. For smaller values of x, the R_{cnt} TC would be dominant and a negative overall TC will be obtained, while for larger values of x the R_{core} TC would be dominant and a positive overall TC will be achieved.

To be able to differentiate between R_{long} and R_{short}, any long resistor R_{tot} with sufficiently large x which results in a positive TC resistor is referred to as R_{long}. In our example, if $x > 3.15$, then the resistor is classified as R_{long}. On the other hand, if x is such that the TC of the resistor is negative ($x < 3.15$ for our example), then the resistor is referred to as R_{short}. In essence, R_{long} has P-TC and R_{short} has N-TC. However, this approach has two main limitations: (1) Since n must be an integer, the value of the designed resistor will most likely be different from the desired value. (2) R_{tot} consists of the resistor structures with different lengths (i.e. R_{long} and R_{short} components), thus it does not have a structured layout and is also sensitive to process. Therefore to address these shortcomings, we propose another resistor structure that resolves the aforementioned issues and furthermore makes the design procedure simpler and more practical. This modified structure is based on using identical resistor components and in the following section, we describe the steps that has led to this structure.

3 Analysis and design of an arbitrary resistor with desired TC

Consider an R_{tot} shown in Fig. 1 (as presented in [29], it has been designed to have a near Z-TC): the core part of R_{long} can be divided into smaller sizes and added to the resistive core part of R_{short} components, such that all the components (R_{long} and all the resistors in R_{short}) have the same length. Owing to this re-distribution, the temperature behaviour of R_{tot} should remain the same, since it still consists of the same amount of core resistor with P-TC and contact resistor with N-TC. This uniform resistor structure will minimise the impacts of process on the R_{tot}. With this rearrangement, any given resistor can be laid out with N uniform resistors with a length of $X/N \times L_{min}$, as shown in Fig. 2. Note that, $X = N \times x$, that is, $x = X/N$.

Assuming such a multi-finger resistor structure, by substituting X and N into (1), the R_{tot} can be written as follows

$$R_{tot} = X \times \left(R_{core} \times \frac{L_{min}}{W_{min}} \right) + N \times \left(2 \times \frac{R_{cnt}}{W_{min}} \right) \quad (4)$$

where L_{min} and W_{min} are the minimum length and width of the

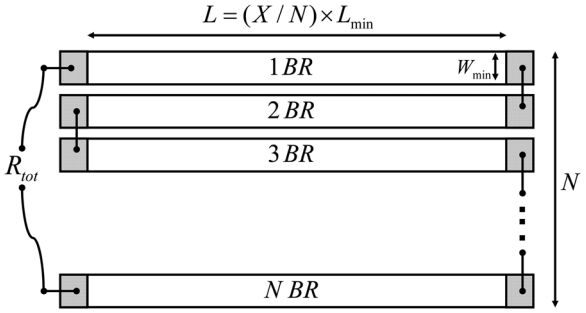

Fig. 2 *R_{tot} example; series combination of N balance resistors (BRs) with the same length factor of X/N*

core resistor. Multiplying both sides of (4) by W_{min}, we obtain

$$R_{tot} \times W_{min} = X \times R_{core} \times L_{min} + 2N \times R_{cnt} \quad (5)$$

Recall from Table 1, a unit resistor $R_{u.core}$ denotes a minimum-size unit resistor, that is, $R_{core} \times L_{min}$. Also, a unit contact resistor $R_{u.cnt}$ is denoted by $2 \times R_{cnt}$ (since each unit resistor has two contacts) and a unit total resistor $R_{u.tot}$ is defined as $R_{tot} \times W_{min}$. Using these notations, we rewrite (5) as

$$R_{u.tot} = X \times R_{u.core} + N \times R_{u.cnt} \quad (6)$$

Equation (6) can be rewritten as

$$X = \frac{R_{u.tot} - N \times R_{u.cnt}}{R_{u.core}} \quad (7)$$

This equation relates X and N based on the value of the desired resistance. Note that given a technology and the desired value of the resistor that we want to design, the values of $R_{u.core}$, $R_{u.cnt}$ and $R_{u.tot}$ are known and fixed. Thus, (7) provides a known relationship between X and N.

Another relation between X and N can be obtained based on the requirement on the temperature dependence. More specifically, the TC of $R_{u.tot}$ in (6) is

$$X \times TC_{core} \times R_{u.core} + N \times TC_{cnt} \times R_{u.cnt} \quad (8)$$

To achieve a (near) Z-TC, we require (note that the desired TC can be a negative, zero or positive number, however, without loss of generality, we have assumed that a (near) Z-TC is desirable)

$$X \times TC_{core} \times R_{u.core} + N \times TC_{cnt} \times R_{u.cnt} = 0 \quad (9)$$

Equation (9) can be rewritten as

$$XN = -\frac{TC_{cnt} \times R_{u.cnt}}{TC_{core} \times R_{u.core}} \quad (10)$$

Given that the TCs of contact and core resistors have opposite signs, the right-hand side of (10) is positive. We denote this value for which the positive and negative TCs of the resistor components balance each other as the balance factor (BF), that is

$$XN = \left| \frac{TC_{cnt} \times R_{u.cnt}}{TC_{core} \times R_{u.core}} \right| = BF \quad (11)$$

Note that given a technology, BF is a fixed number and can be calculated from the process parameters provided by the foundry (similar to those given in Table 1). Equation (11) can be rewritten as

$$X = N \times BF \tag{12}$$

This equation relates X and N for a (near) Z-TC resistor. Thus, (7) and (12) provide a system of two equations of two unknowns and can be solved for X and N.

Note that since R_{tot} has a near Z-TC consisting of identical resistor units, every resistor unit must have near Z-TC. Thus, intuitively, each of these resistor units has to have a length (i.e. X/N) that is exactly equal to BF. In other words, the R_{tot} consists of N resistor units each of length $X/N \times L_{\min}$ and having a near Z-TC. Therefore, we call this near Z-TC resistor unit balanced resistor (BR).

For example, suppose that we want to design a 15 kΩ resistor with a (near) Z-TC. From Table 1 we have, $R_{u.\text{tot}} = 15 \times 0.4 = 6$ Ω·μm and

$$\text{BF} = \left| \frac{\text{TC}_{\text{cnt}} \times R_{u.\text{cnt}}}{\text{TC}_{\text{core}} \times R_{u.\text{core}}} \right| = 3.15 \tag{13}$$

After solving for X and N from (7) and (12), we have $N = 4.12$ and $X = 12.98$. However, since N is a number of resistor units, it has to be an integer. Thus, for $N = 4$ ($N = 5$), X becomes 12.6 (15.75), hence introducing an error of (12.6–12.98)/12.98 = –2.9% (21.3%) in the value of the resistor. The designed resistor will be $R_{u.\text{tot}} = 14.6$ kΩ (18.2 kΩ) instead of 15 kΩ.

Thus, in this structure (as compared to the structure previously presented in [29] which is based on R_{long} and R_{short}), all resistor units are identical and therefore have the same temperature behaviour. Furthermore, this structure with identical unit resistors is more layout-friendly. However, with this approach, one still cannot design an R_{tot} with an arbitrary value and there will be some error due to the requirement of N being a positive integer number. In what follows, we address the design problem of how to implement an arbitrary (near) Z-TC resistor with minimal (ideally zero) error in its value.

Table 2 Algorithm results for computing all possible residual resistor values based on previously constructed resistor combinations with a 5% precision

$R_s(k)$	$k = 1$	$k = 2$	$k = 3$	$k = 4$
$s = 1$	1.00	—	—	—
$R_1(k)$	BR	—	—	—
$s = 2$	0.50	—	—	—
$R_2(k)$	$R_1(1) \| \| R_1(1)$	—	—	—
$s = 3$	0.33	—	—	—
$R_3(k)$	$R_1(1) \| \| R_2(1)$	—	—	—
$s = 4$	0.25	—	—	—
$R_4(k)$	$R_1(1) \| \| R_3(1)$	—	—	—
$s = 5$	0.20	0.83	—	—
$R_5(k)$	$R_1(1) \| \| R_4(1)$	$R_2(1) + R_3(1)$	—	—
$s = 6$	0.16	0.45	0.75	0.66
$R_6(k)$	$R_1(1) \| \| R_5(1)$	$R_1(1) \| \| R_5(2)$	$R_2(1) + R_4(1)$	$R_3(1) + R_3(1)$
$s = 7$	0.14	0.42	0.70	0.58
$R_7(k)$	$R_1(1) \| \| R_6(1)$	$R_1(1) \| \| R_6(3)$	$R_2(1) + R_5(1)$	$R_3(1) + R_4(1)$
$s = 8$	0.36	0.95	—	—
$R_8(k)$	$R_1(1) \| \| R_7(4)$	$R_2(1) + R_6(2)$	—	—
$s = 9$	0.64	0.92	—	—
$R_9(k)$	$R_2(1) + R_7(1)$	$R_2(1) + R_7(2)$	—	—
$s = 10$	0.86	—	—	—
$R_{10}(k)$	$R_2(1) + R_8(1)$	—	—	—
$s = 11$	0.09	—	—	—
$R_{11}(k)$	$R_4(1) \| \| R_7(1)$	—	—	—
$s = 12$	—	—	—	—
$R_{12}(k)$	—	—	—	—
⋮	—	—	—	—
$s = 21$	—	—	—	—
$R_{21}(k)$				
$s = 22$	0.04	—	—	—
$R_{22}(k)$	$R_{11}(1) \| \| R_{11}(1)$	—	—	—

3.1 (Near) Z-TC resistor with an arbitrary value using parallel/series-combinations algorithm

Let us first find the minimum possible value of BR available in a given technology. Given that

$$\text{BF} = \left| \frac{\text{TC}_{\text{cnt}} \times R_{u.\text{cnt}}}{\text{TC}_{\text{core}} \times R_{u.\text{core}}} \right| \tag{14}$$

from (7), (12) and (14), we have

$$N = R_{u.\text{tot}} / \left(R_{u.\text{cnt}} - R_{u.\text{cnt}} \frac{\text{TC}_{\text{cnt}}}{\text{TC}_{\text{core}}} \right) \tag{15}$$

For the process used in this work, substituting $R_{u.\text{cor}}$ and $R_{u.\text{cnt}}$ in kΩ, we obtain $N = R_{u.\text{tot}}/1.46$ or $R_{u.\text{tot}} = 1.46N$. Since $R_{u.\text{tot}} = R_{\text{tot}} \times W_{\min}$, we can derive R_{tot} as a function of N for $W_{\min} = 0.4$ μm as follows

$$R_{\text{tot}} = (1.46/0.4) \times N = 3.65 \times N \tag{16}$$

From (16), one can obtain possible values for structures made of series combination of N BRs.

If the specific resistor values given by (16) can be used in a design, then no additional design step is required. However, if a different value is desired, which is typically the case, then the following approach can be applied.

Since the minimum BR increment is 3.65 kΩ (for $N = 1$ and near Z-TC), we need a procedure to design an smaller resistor in the range of 0–3.65 kΩ, so that it can be added to any series combination of the BR building blocks (16) to cover the full range of resistances. One possibility is to use parallel combination of these BRs to create the smaller residual resistor. There are many different ways to implement such smaller resistor, however, many are *ad hoc* methods and will not necessarily result in an optimal configuration (in a sense of number of resistors used). To achieve the optimal configuration with the least number of BRs, we can use a dynamic programming algorithm [30] and efficiently find all possible values for such residual resistors with a given error bound (as percentage of BR). Given the specific percentage error of e, the algorithm considers separate intervals of $[p \times e, (p+1) \times e)$ for all $0 \le p \le 1/e - 1$ and finds a specific series/parallel combination of BRs with minimum number of resistor building blocks whose value is inside each interval. For instance, if $e = 5\%$, there are 20 intervals of the form $[p \times 0.05, (p+1) \times 0.05)$ with $0 \le p \le 19$, and thus the algorithm finds 20 resistors each located in a different interval, so that, there is one value within each interval. The algorithm is as follows. In this discussion, s, i, j, k, k' and k'' are all positive integers.

We define $R_1(1) = \text{BR}$ and for the integer number $s \ge 2$, we define R_s as the set of resistors, where each element of the set, $R_s(k)$, has a value that is less than BR, and each element is implemented using series and/or parallel combination of

doi: 10.1049/iet-cds.2012.0126

exactly s BR resistors. Furthermore, R_s only includes the resistors which are not in any R_j where $j < s$. For example, R_2 is a set of all combinations of two BR resistors. Since there are only two possibilities, parallel or series combination of two BRs, and the elements of R_2 are required to be smaller than BR, there will be only one element in R_2, whose value relative to BR is 0.5 (implemented by combining two BR components in parallel). We compute all possible elements of R_s in a bottom-up scheme (i.e. the elements of R_s are series or parallel combinations of two elements, one from R_i and the other from R_{s-i}, where $0 < i \leq s/2$), shown in Fig. 3*a*, according to the following formula

$$R_s(k) = \begin{cases} R_i(k') + R_{s-i}(k''), & \forall i: 0 < i \leq s/2 \\ & \forall \{k, k', k''\} \geq 0 \\ \text{OR} & \\ & \forall i: 0 < i \leq s/2 \\ R_i(k') \parallel R_{s-i}(k''), & \forall \{k, k', k''\} \geq 0 \end{cases}$$

In order to avoid any duplication, we use a hash table [30] and store the values that have been already calculated. For example, given a desired precision of 5% again, the proposed algorithm checks different configurations of such BR-based resistors until it finds exactly one resistor for each of the 20 intervals.

Table 2 shows the result of the proposed algorithm for computing all 20 residual resistor values for a 5% precision. Note that some of R_i sets are empty sets. It also provides information on how each resistor has been implemented based on the previously calculated resistors. For example, for designing a 0.42 BR combination, refer to $R_7(2)$, we use a parallel combination of $R_6(3)$ and $R_1(1)$, where $R_6(3)$ is the series combination of $R_4(1)$ and $R_2(1)$. The structure is shown in Fig. 3*b*.

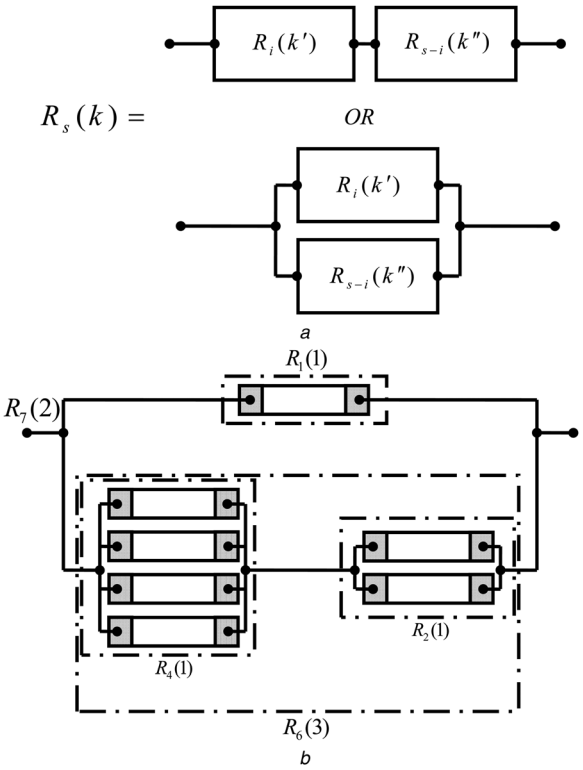

Fig. 3 *Z-TC resistor example using parallel/series-combinations algorithm*

a $R_s(k)$ is constructed by either series or parallel combination of two elements from previous sets

b Reconstructed $R_7(2)$ by parallel combination of $R_1(1)$ and $R_6(3)$ which in turn have been reconstructed based on Table 2. All building block resistors have the same value of a unit BR

We now provide an example: Assume that we want to design the same 15 kΩ resistor that we discussed earlier. Further, assume that the required precision is 5% of BR (i.e. $0.05 \times 3.65\ \text{k}\Omega = 182.5\backslash\Omega$). As a first step, one can chose a closest value smaller than the given R_{tot} from (16), which in this case is 14.60 (using for $N = 4$ in (16)). By combining four BRs in series, we obtain 14.60 kΩ. Therefore, we need to find $15 - 14.6 = 0.4\ \text{k}\Omega$ residual resistor, using the proposed algorithm. 0.4 kΩ is 0.11 of BR (3.65 kΩ), hence we can use algorithm results listed in Table 2 to find the close value to 0.11, which is $R_{11}(1) = 0.09$. Therefore one can implement R_{tot} as a series combination of four BRs in series with 11 BRs in parallel. The final value turns out to be $4 \times 3.65 + 0.09 \times 3.65 = 14.93\ \text{k}\Omega$ with an error of (14.93–15)/15 = 0.5% (or approximately 2% of BR which is within the desired 5% precision).

If a higher precision for R_{tot} is desired, then one needs to use the same algorithm to find a larger number of residual resistors. For example, for a precision of 1% with respect to BR, 100 residual resistors have to be found. Using the proposed algorithm, one can efficiently find the optimal residual resistor configuration (in a sense of number of BR elements used) for any desired precision. The proposed algorithm provides a technique to design any given resistor with an arbitrary unit resistor. Here, we use this technique to design (near) Z-TC resistors. Without loss of generality, this technique can be extended for designing a resistor with a desired TC.

3.2 Z-TC resistor with an arbitrary value by changing resistor width, W

The algorithm proposed in the previous subsection is useful when it is desired to keep the width of each resistor block constant (e.g. in this paper, we assumed minimum width structures). Note that the temperature behaviour of the proposed resistor which consists of BRs is independent of the W of its components. This is due to the fact that the BF found in (11) depends on both $R_{u.\text{core}}$ and $R_{u.\text{cnt}}$, while these unit resistors (based on (2)) are independent of the W, resistor width. W affects both $R_{u.\text{core}}$ and $R_{u.\text{cnt}}$ in the same way and since $R_{u.\text{core}}$ has P-TC and $R_{u.\text{cnt}}$ has N-TC, thus temperature-wise the effect of W is cancelled out. Although the temperature behaviour of the proposed resistor structure is independent of its W, the value of the resistor is indeed a function of W (refer to (2)). Thus, one can increase (decrease) the width of all BR building blocks to decrease (increase) the value of R_{tot} without changing the TC of the resistor structure. This fact leads us to a simpler design procedure without the need to use the algorithmic design proposed earlier.

3.3 Main proposed design procedure

The proposed procedure to implement any arbitrary resistor with (near) Z-TC behaviour is presented here. Note that the procedure is general and can be applied to any TC; however, without loss of generality, we are focusing on (near) Z-TC structures. Let us consider the same design

example of implementing a 15 kΩ resistor that we discussed earlier. Based on (15), if we use an arbitrary $W = W_{min} + \Delta W$, we can derive

$$N = \frac{R_{tot} \times (W_{min} + \Delta W)}{1.46} \quad (17)$$

where in our process $W_{min} = 0.4$. The corresponding resistor structure is the same as what is shown in Fig. 2 with $W = W_{min} + \Delta W$ instead of W_{min}.

To design and implement a (near) Z-TC $R_{tot} = 15$ kΩ, using resistor components with width of W_{min}, the raw value for N was calculated to be 4.12. By properly choosing ΔW, one can adjust N to be an integer, for example, 5 in this case where a new W can be found to be $5 \times 1.46/15 \simeq 0.49$ μm. That is, a ΔW of 0.09 μm is required. As a side note, by increasing the W from 0.4 μm to 0.49 μm, a 14.90 kΩ resistor is achieved. The value of the resistor can be further refined if finer width adjustments are possible in the technology. Using $W = 0.49$ μm introduces an error of about 100 Ω as compared to the target resistor, 15 kΩ which translates to ~0.7% error. Since the fine tuning of the value is achieved by adjusting the width of the building blocks, the number of overall resistor blocks used is generally less than that of the case when the width of all resistor building blocks is fixed (which was the case for the proposed algorithm in Section 3.1).

It is worthwhile to mention that instead of increasing the W of all N BRs shown in Fig. 2, one can only increase the W of one BR component and keep the rest intact.

In summary, the proposed design procedure is as follows: to implement an arbitrary resistor with (near) Z-TC, we would first choose the closest available BR whose value is larger than the desired resistor using (16). For instance, if the goal is to design a 20 kΩ resistor, we choose 21.90 kΩ structure which consists of $N = 6$ BR components. Then, we increase the width of all, some or only one of these $N = 6$ BR building blocks to achieve the desired resistance.

Note that the proposed design procedure is general and one can also design and implement a resistor with an arbitrary positive or negative TC value by setting the (9) equal to the desired TC rather than zero. The design strategy is the same as shown in Fig. 2, the only difference is to choose different length for the resistor components in series combination; in other words, we still use the same structure, but for N-TC the resistor lengths will be less than BF (the resistor components will be R_{short}), and for P-TC the resistor lengths will be more than BF (the resistor components will be R_{long}). The positive and negative TC range of such resistor is limited by the TC of core and contact resistors, TC_{core} and TC_{cnt}, which are provided by the specific target technology. As a proof-of-concept of the proposed technique, we have designed and implemented several different resistor structures. The simulation and measurement results are provided in the following section.

4 Simulation and measurement results

Based on the design technique proposed above, we have simulated and implemented several different resistor structures with Z-TC, N-TC and P-TC. All the simulation and measurement results provided in this section are over the temperature range of 25–200°C. The simulations are performed in Cadence Virtuoso Spectre circuit simulator and use foundry provided models.

First, we provide the results for a BR of 1, 10 and 100 kΩ to prove the validity of the proposed technique. Then, we investigate the role of different width size of a given BR on its temperature behaviour for different number of series resistor components, N. In this case, we use yet another BR value, that is, ~8 kΩ. Finally, we compare the temperature behaviour of 10 and 100 kΩ R_{tot} from different structures: BR, R_{short} and R_{long}. In this work, all resistors have been designed and implemented using the structure shown in Fig. 2.

During the measurements, for each resistor, we applied between 50 and 150 different sample currents and measured the voltage across the resistor for each current at the given temperature. The resistor value for each temperature has been calculated by fitting a line into measured current/voltage data. The measurements are done on three different test chips and at 25, 75, 125, 175 and 200°C.

4.1 Temperature stability of BRs in the range of 1–100 kΩ

The simulation and measurement results presented in Fig. 4 provide the temperature stability of three different BRs in a range of 1–100 kΩ. Note that there is a good match between the simulation and measurement results. The values of BR structures are arbitrarily chosen to show the validity of the method, however, the performance is not limited to these values. Note that for larger size resistors, for example, 1 MΩ, one can use a series combination of the above resistors (e.g. 10 × 100 kΩ BR structure) and achieve the same temperature stability. Also, for smaller size resistors, for example, 100 Ω for example, one can use a parallel combination of such resistors (e.g. 10 × 1 kΩ BR structure).

4.2 Temperature stability of an ~8 kΩ resistor with different width BRs

In this section, we investigate the effect of the width of the resistor components on the temperature behaviour of the proposed BR structure. As expected, the measurements confirm that the temperature stability of the proposed

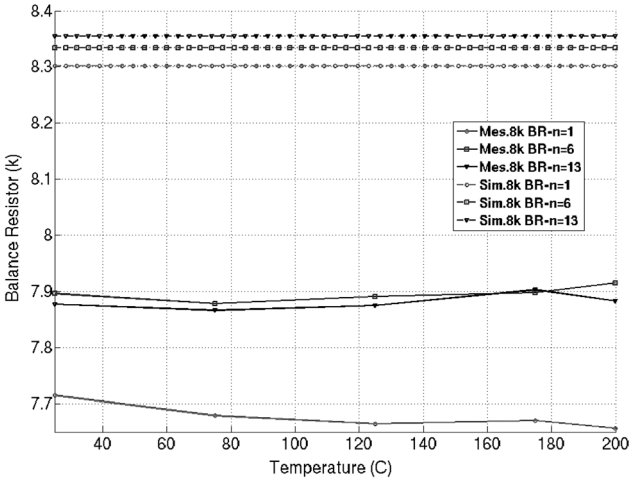

Fig. 4 *Simulation and measurement results for BRs of 1, 10, 100 kΩ over the temperature range of 25–200°C*

The measured TCs (ppm/°C) are +62.9, −19.4 and −56.7, respectively

doi: 10.1049/iet-cds.2012.0126

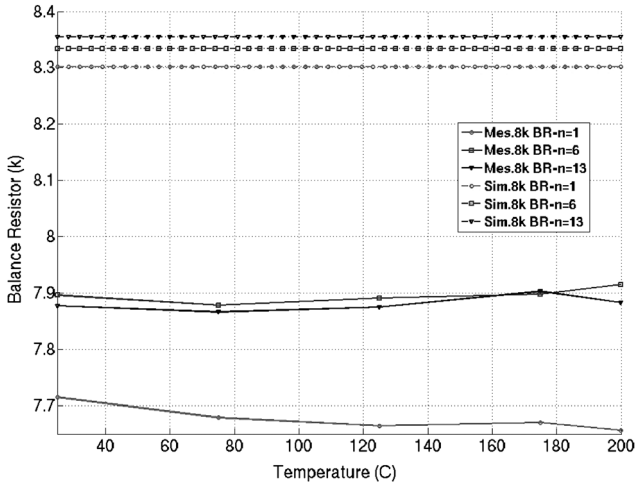

Fig. 5 *Simulation and measurement results for a ∼8 kΩ BR with different width size (N = 1, 6 and 13) over the temperature range of 25–200°C*

The measured TCs (ppm/°C) are −41.4, +26.4 and +30.8, respectively

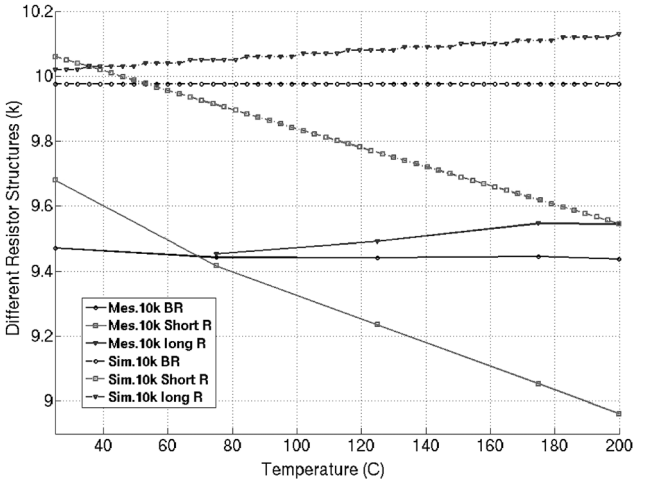

Fig. 6 *Simulation and measurement results for a 10 kΩ resistor with different structures (BR, R_{short} and R_{long}) over the temperature range of 25–200°C*

Measurements are done on three different test chips, however, the variation at each point is less than 10 Ω and thus are masked by the marker. Note that the measured TC (ppm/°C) of the BR structure which is supposed to have a (near) Z-TC is −19.4

resistor structure is independent of the width of its building blocks.

Fig. 5 shows the simulation and measurement results of an ∼8 kΩ BR with three different width size. In essence, we designed three BRs with $N = 1$, 6 and 13 and for larger number of N, we also increased the width so that the total amount of BR structure remains about the same ∼8 kΩ.

Comparing the measurements and simulations, there are some errors in the total amount of all three resistors. The one with $N = 1$ introduces a larger error, whereas the other two ($N = 6$ and 13) show about the same error. This extra error can be attributed to the impact of process variation during the fabrication, since $N = 1$ structure is highly process-dependent, whereas the other two are more robust due to multiple finger structure. Therefore comparing $N = 6$ with $N = 13$ BR structure, they both provide about the same temperature behaviour over the temperature range of 25–200°C. Note that in all cases the value of the resistor is approximately temperature-independent (N-TC behaviour).

4.3 Comparing 10 kΩ BR, R_{short} and R_{long} structures

The simulation and measurement results in Fig. 6 present the temperature behaviour of a 10 kΩ resistor with three different structures, BR, R_{short} and R_{long}. Supporting the proposed technique, both simulation and measurement results confirm that the R_{short} shows an N-TC behaviour since the TC of contacts is dominant as compared to the core resistor TC, while the BR obtains (near) Z-TC and the R_{long} shows a P-TC behaviour since the core resistor TC is dominant as compared to the TC of contacts. These results are also listed in Table 3.

Table 3 TC of a 10 kΩ resistor with different structures (BR, R_{short} and R_{long}) over the temperature range of 25–200°C calculated based on both simulation and measurement results

10 kΩ	*BR*	R_{short}	R_{long}
TC_{sim} ppm/°C	−0.041	−293	+61
TC_{mes}/°C	−19.4	−411	+73

4.4 Comparing 100 kΩ BR, R_{short} and R_{long} structures

The simulation and measurement results shown in Fig. 7 present the temperature behaviour of a 100 kΩ resistor again with three different structures, BR, R_{short} and R_{long}. The simulation results illustrate the same temperature behaviour compared with the results for a 10 kΩ resistor

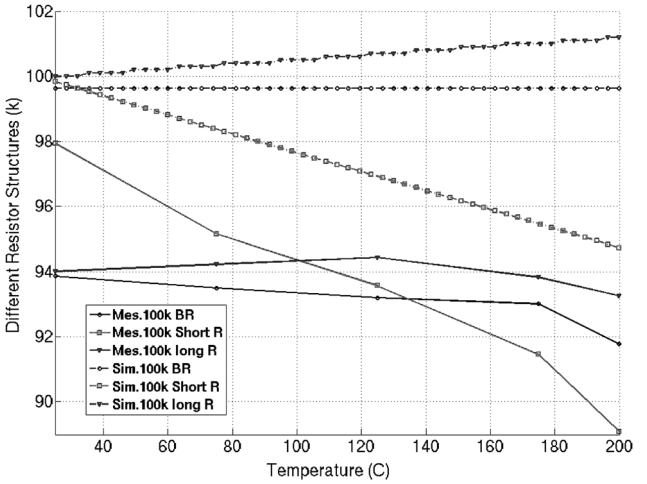

Fig. 7 *Simulation and measurement results for a 100 kΩ resistor with different structures (BR, R_{short} and R_{long}) over the temperature range of 25–200°C*

Measurements are done on three different test chips, however, the variation at each point is less than 100 Ω and thus are masked by the marker. The measured TC (ppm/°C) of the BR structure, which is supposed to have a (near) Z-TC is −56.7

shown in Fig. 6. This trend confirms the validity of the proposed technique for different resistor values. Note that the measurement results show a bend, that is, steeper drop, at high temperature (beyond 175°C) for all three large value resistor structures (i.e. 100 kΩ resistors in this work). The

bend can be attributed to the dangling bond effect of polysilicon resistors, which appears and dominates at about 200°C and it reduces the resistance value of the polysilicon materials [31].

5 Conclusion

A technique for implementing monolithic resistors with a desired TC over a wide temperature range is presented. The technique is based on taking advantage of resistor contacts that has an opposite TC as compared to the TC of the resistor core itself. The main design goal is to find a specific length factor based on the proposed technique for implementing a given resistor R_{tot} with a desired TC. Finding this length factor, one can use the proposed resistor structure consisting of identical resistor components with the same length factor to implement the R_{tot}. These identical resistors can be chosen to be R_{long}, BR or R_{short}, depending on the desired TC values, which are P-TC, (near) Z-TC or N-TC, respectively. Several resistor structures in the range of 1–100 kΩ have been simulated and implemented in a 0.13 μm CMOS technology. The simulation and measurement results over the temperature range of 25–200°C confirm the validity of the proposed technique. The technique is general and can be applied to any technology (aside from the 0.13 μm CMOS technology used in this work) in which core and contact components of resistors have opposite TC. The proposed technique to implement (near) Z-TC resistors has been used in a 1-MHz relaxation oscillator to stabilise the output frequency of the oscillator over a wide temperature range [32].

6 References

1 Kousai, S., Hamada, M., Itakura, T.: 'A 19.7 MHz fifth-order active-RC Chebychev LPF draft IEEE 802.11n with automatic quality factor tuning scheme', *IEEE J. Solid-State Circuits*, 2007, **SC-42**, pp. 2326–2337

2 Vasilopoulos, A., Vizilaios, G., Theodoratos, G., Papananos, Y.: 'A low-power reconfigurable integrated active-RC filter with 73 dB SFDR', *IEEE J. Solid-State Circuits*, 2006, **SC-41**, pp. 1997–2008

3 Durham, A.M., Hughes, J.B., Redman-White, W.: 'Circuit architectures for high linearity monolithic continuous time filtering', *IEEE Trans. Circuits Syst.*, 1992, **CAS-39**, (Part II), pp. 651–657

4 Durham, A.M., Redman-White, W., Hughes, J.B.: 'High-linearity continuous time filter in 5-V VLSI CMOS', *IEEE J. Solid-State Circuits*, 1992, **SC-27**, pp. 1270–1276

5 Razavi, B.: 'Design of analog CMOS integrated circuits' (McGraw-Hill, 2001)

6 Yu, X.: 'High-Temperature bulk CMOS integrated circuits for data acquisition'. PhD thesis, Case Western Reserve University, 2006

7 Yu, X., Garverick, S.L.: 'Mixed-signal, 275°C instrumentation amplifier in bulk CMOS'. IEEE Custom Integrated Circuits Conf., September 2005, pp. 641–644

8 Sadeghi, N., Mirabbasi, S., Bennington, C.P.J.: 'A 2.5 V 0.13 μm CMOS amplifier for a high-temperature sensor system'. IEEE Int. NEWCAS-TAISA Conf., June 2009, pp. 263–266

9 Davis, C., Finvers, I.: 'A 14-bit high-temperature ΣΔ modulator in standard CMOS', *IEEE J. Solid-State Circuits*, 2003, **38**, (6), pp. 976–986

10 Barnett, R., Liu, J.: 'A 0.8 V 1.52 MHz MSVC relaxation oscillator with inverted mirror feedback reference for UHF RFID'. IEEE Custom Integrated Circuits Conf., 2006, pp. 769–772

11 Audy, J.M.: 'Bandgap voltage reference circuit and method with low TCR resistor in parallel with high TCR and in series with low TCR portions of tail resistor'. U.S. Patent 5,291,122, March 1994

12 Lu, J., Wang, Y., Xu, N., Gao, M.: 'Temperature compensation in bootstrapped current reference source'. IEEE Conf. Electron Devices Solid-State Circuits, 2003, pp. 491–494

13 Nachrodt, D., Paschen, U., Have, A.T., Vogt, H.: 'Ti/Ni(80%)Cr(20%) thin-film resistor with a nearly zero temperature coefficient of resistance for integration in a standard CMOS process', *IEEE Electron Device Lett.*, 2008, **29**, (3), pp. 212–214

14 Ito, H., Nagasaka, T.: 'Resistor circuit with reduced temperature coefficient of resistance'. U.S. Patent 5,506,494, April 1996

15 Zandman, F., Szwarc, J.: 'Precision power resistor with very low temperature coefficient of resistance'. U.S. Patent 4,677,413, June 1987

16 Shah, R., Hughey, S.L.: 'Method of making zero temperature coefficient of resistance resistors'. U.S. Patent 4,579,600, April 1986

17 Matsuura, M.: 'Film resistor having a reduced temperature coefficient of resistance'. U.S. Patent 4,145,470, March 1979

18 Jones, W.K.: 'Zero temperature coefficient of resistance bi-film resistor'. U.S. Patent 4,104,607, August 1978

19 Xiangning, F., Da, C., Yangyang, F.: 'A switch controlled resistor based CMOS PGA with DC offset cancellation for WSN RF chip'. Int. Symp. Signals Systems and Electronics (ISSSE), 2010, vol. **1**, no., pp. 1–4, see also pp. 17–20

20 Jiraseree-amornkun, A., Worapishet, A., Klumperink, E., Nauta, B., Surakampontorn, W.: 'Theoretical analysis of highly linear tunable filters using switched-resistor techniques', *IEEE Trans. Circuits Syst. I: Reg. Pap.*, 2008, **55**, (11), pp. 3641–3654

21 Hsu, C.C., Wu, J.T.: 'A highly linear 125-MHz CMOS switched-resistor programmable-gain amplifier', *IEEE J. Solid-State Circuits*, 2003, **38**, (10), pp. 1663–1670

22 Bergeron, D., Stephens, G.B.: 'Voltage compensation of temperature coefficient of resistance in an integrated circuit resistor'. U.S. Patent 4,229,753, October 1980

23 Banerjee, R.: 'Low temperature coefficient resistor'. U.S. Patent 6,960,979 B2, November 2005

24 Banerjee, R.: 'Low temperature coefficient resistor'. U.S. Patent 6,621,404 B1, September 2003

25 Laraia, J.M.: 'Circuits and methods for providing a current reference with a controlled temperature coefficient using a series composite resistor'. U.S. Patent 6,351,111, February 2002

26 Wit, M.d.: 'Temperature independent resistor'. U.S. Patent 5,448,103, September 1995

27 Hayasaka, I.: 'Method of manufacturing a resistor having a low temperature coefficient'. U.S. Patent 3,979,823, September 1976

28 Hayasaka, I.: 'Resistor with low temperature coefficient'. U.S. Patent 3,970,983, July 1976

29 Sadeghi, N., Mirabbasi, S.: 'A technique for implementing monolithic resistors with near-zero temperature coefficient'. IEEE Canadian Conf. Electrical and Computer Engineering, May 8, 2011, pp. 1292–1295

30 Cormen, T.H., Leiserson, C.E., Rivest, R.L., Stein, C.: 'Introduction to algorithms' (MIT Press, Cambridge, MA, 2001)

31 Nakabayashi, M., Ikegami, M., Daikoku, T.: 'Influence of hydrogen on electrical characteristics of poly-Si resistor', *Jpn. J. Appl. Phys.*, 1993, **32**, (9A), pp. 3734–3738

32 Sadeghi, N., Sharif-Bakhtiar, A., Mirabbasi, S.: 'A 0.007 mm^2 108 ppm/°C 1-MHz relaxation oscillator for high-temperature applications up to 180°C in 0.13 μm CMOS'. To appear in IEEE Transactions on Circuits and Systems I (TCAS-I), accepted in September 2012

doi: 10.1049/iet-cds.2012.0126